Notice of Allowability	Application No.	Applicant(s)	
	09/882,417	CHAMBERS ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *appeal brief filed on 04/22/05*.

2. ☒ The allowed claim(s) is/are *1-15*.

3. ☒ The drawings filed on *15 June 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

1. Claims **1-15** have been allowed.

As per claim 1:

The prior art, Gonzales et al. (U.S. PN: 6,101,614) record teach a method of transferring data of a system of a read channel data recorded or stored on memories for performing a Reed-Solomon decoding including error correction whereby the system includes an input buffer, a bus, a Reed-Solomon decoder and de-scrambling controller. Further, Gonzales et al. teach a memory controller comprising a memory interface to read data from an address in memory indicated by a memory read request, an error checking and correcting (ECC) logic coupled to receive the data read from the address in memory whereby the ECC is being configured to detect whether the data has a correctable error and to issue an error signal and correct the correctable error to generate corrected data if the data has a correctable error, a control logic (control unit) coupled to receive the error signal from the ECC whereby the control logic is being configured to tag the memory read request in response to the error signal to indicate that the data has the correctable error, and write the corrected data back to the address in memory indicated by the tagged memory read request (see col. 8, lines 37-49 claim 8). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from

said memory subsystem and to write a corrected version of said data within said memory subsystem. Consequently, claim 1 is allowed over the prior art.

Claims **2-5,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 6:

The prior art, Gonzales et al. (U.S. PN: 6,101,614) record teach a method of transferring data of a system of a read channel data recorded or stored on memories for performing a Reed-Solomon decoding including error correction whereby the system includes an input buffer, a bus, a Reed-Solomon decoder and de-scrambling controller. Further, Gonzales et al. teach a memory controller comprising a memory interface to read data from an address in memory indicated by a memory read request, an error checking and correcting (ECC) logic coupled to receive the data read from the address in memory whereby the ECC is being configured to detect whether the data has a correctable error and to issue an error signal and correct the correctable error to generate corrected data if the data has a correctable error, a control logic (control unit) coupled to receive the error signal from the ECC whereby the control logic is being configured to tag the memory read request in response to the error signal to indicate that the data has the correctable error, and write the corrected data back to the address in memory indicated by the tagged memory read request (see col. 8, lines 37-49 claim 8). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a control unit is configured to store an indication in said storage unit that said data corresponding to said memory read request is erroneous; and wherein said control unit is further configured to subsequently detect said indication in said storage unit and to responsively perform a subsequent read of said data from

said memory subsystem and to write a corrected version of said data within said memory subsystem. Consequently, claim 6 is allowed over the prior art.

Claims **7-10,** which is/are directly or indirectly dependent/s of claim 6 are also allowable over the prior art of record.

As per claim 11:

The prior art, Gonzales et al. (U.S. PN: 6,101,614) record teach a method of transferring data of a system of a read channel data recorded or stored on memories for performing a Reed-Solomon decoding including error correction whereby the system includes an input buffer, a bus, a Reed-Solomon decoder and de-scrambling controller. Further, Gonzales et al. teach a memory controller comprising a memory interface to read data from an address in memory indicated by a memory read request, an error checking and correcting (ECC) logic coupled to receive the data read from the address in memory whereby the ECC is being configured to detect whether the data has a correctable error and to issue an error signal and correct the correctable error to generate corrected data if the data has a correctable error, a control logic (control unit) coupled to receive the error signal from the ECC whereby the control logic is being configured to tag the memory read request in response to the error signal to indicate that the data has the correctable error, and write the corrected data back to the address in memory indicated by the tagged memory read request (see col. 8, lines 37-49 claim 8). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious storing an indication that said data corresponding to said memory read request is erroneous; and subsequently detecting said indication and responsively performing a subsequent read of said data from said memory subsystem and writing a corrected version of said data within said memory subsystem.

Claims **12-15,** which is/are directly or indirectly dependent/s of claim 11 are also allowable over the prior art of record.

Any comment considering necessary by the applicant must be submitted to near than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reason for Allowance".

Conclusion

2. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100